In The Claims

Please cancel claims 1-55 and add new claims 56-83.

56. (new) A semiconductor device comprising:

a semiconductive substrate;

an inner dielectric layer over the substrate, the inner dielectric layer comprising an oxidized alloy of at least two metals in a perovskite-type crystalline structure; and

an outer dielectric layer over the inner dielectric layer, the outer dielectric layer comprising an oxide of a selected material, such selected material being generally passivated against carbon and nitrogen reaction.

57. (new) The semiconductor device of claim 56 wherein the outer dielectric layer is on and in contact with the inner dielectric layer.

58. (new) The semiconductor device of claim 56 further comprising a middle dielectric layer between the inner and outer dielectric layers, the middle dielectric layer comprising an oxidized alloy of at least two metals in a perovskite-type crystalline structure.

59. (new) The semiconductor device of claim 56 wherein the material comprises amorphous silicon, aluminum, or alloys thereof.

60. (new) The semiconductor device of claim 56 wherein the outer dielectric layer has a thickness of from about 0.5 to about 2 nanometers.

61. (new) The semiconductor device of claim 56 wherein at least two of the metals exhibit a substantial difference in chemical affinity for oxygen.

62. (new) The semiconductor device of claim 56 wherein at least one of the at least two metals is selected from the group consisting of Ti, alkaline earth metals, and lanthanide metals.

63. (new) The semiconductor device of claim 56 wherein the oxidized alloy comprises $PbTiO_3$.

64. (new) The semiconductor device of claim 56 wherein the oxidized alloy comprises $PbZr_yTi_{1-y}O_3$.

65. (new) A semiconductor device comprising:

a semiconductive substrate;

an inner dielectric layer over the substrate, the inner dielectric layer comprising an oxidized alloy of at least two metals in a perovskite-type crystalline structure and at least two of the metals exhibiting a substantial difference in chemical affinity for oxygen; and

an outer dielectric layer on and in contact with the inner dielectric layer, the outer dielectric layer comprising an oxide of a material comprising amorphous silicon, aluminum, or alloys thereof and the material exhibiting passivation against carbon and nitrogen reaction.

66. (new) The semiconductor device of claim 65 wherein the device is comprised by an integrated circuit.

67. (new) The semiconductor device of claim 65 wherein the oxide of the material comprises Al_2O_3.

68. (new) The semiconductor device of claim 65 wherein the oxide of the material comprises SiO_2.

69. (new) The semiconductor device of claim 65 wherein the outer dielectric layer has a thickness of from about 0.5 to about 2 nanometers.

70. (new) The semiconductor device of claim 65 wherein at least one of the at least two metals is selected from the group consisting of Ti, alkaline earth metals, and lanthanide metals.

71. (new) The semiconductor device of claim 65 wherein the oxidized alloy comprises $PbTiO_3$.

72. (new) The semiconductor device of claim 65 wherein the oxidized alloy comprises $PbZr_yTi_{1-y}O_3$.

73. (new) An integrated circuit component comprising:

a bulk semiconductive wafer substrate;

an inner dielectric layer over the substrate, the inner dielectric layer comprising an oxidized alloy of at least two metals in a perovskite-type crystalline structure and at least two of the metals exhibiting a substantial difference in chemical affinity for oxygen; and

a passivation layer over the inner dielectric layer, the passivation layer exhibiting passivation against carbon and nitrogen reaction with the inner dielectric layer.

74. (new) The integrated circuit component of claim 73 wherein the component comprises dynamic random access memory.

75. (new) The integrated circuit component of claim 73 wherein the component comprises non-volatile field effect transistor memory.

76. (new) The integrated circuit component of claim 73 wherein the passivation layer is on and in contact with the inner dielectric layer.

77. (new) The integrated circuit component of claim 73 further comprising a middle dielectric layer between the inner dielectric layer and the passivation layer, the middle dielectric layer comprising an oxidized alloy of at least two metals in a perovskite-type crystalline structure.

78. (new) The integrated circuit component of claim 73 wherein the passivation layer comprises amorphous silicon, aluminum, or alloys thereof.

79. (new) The integrated circuit component of claim 73 wherein the passivation layer comprises a dielectric material.

80. (new) The integrated circuit component of claim 73 wherein the passivation layer has a thickness of from about 0.5 to about 2 nanometers.

81. (new) The integrated circuit component of claim 73 wherein at least one of the at least two metals is selected from the group consisting of Ti, alkaline earth metals, and lanthanide metals.

82. (new) The integrated circuit component of claim 73 wherein the perovskite-type crystalline structure comprises $PbTiO_3$.

83. (new) The integrated circuit component of claim 73 wherein the perovskite-type crystalline structure comprises $PbZr_yTi_{1-y}O_3$.